



The diagram shows a semiconductor device 1 with a substrate 2. The substrate contains a grid of alternating N-type and P-type regions. The regions are arranged in columns 4 and 5, and rows 6 and 7. The columns are labeled 7A and 7B. A power supply 15 is connected to the grid. The regions are labeled 4, 5, 6, and 7.

FIG.3

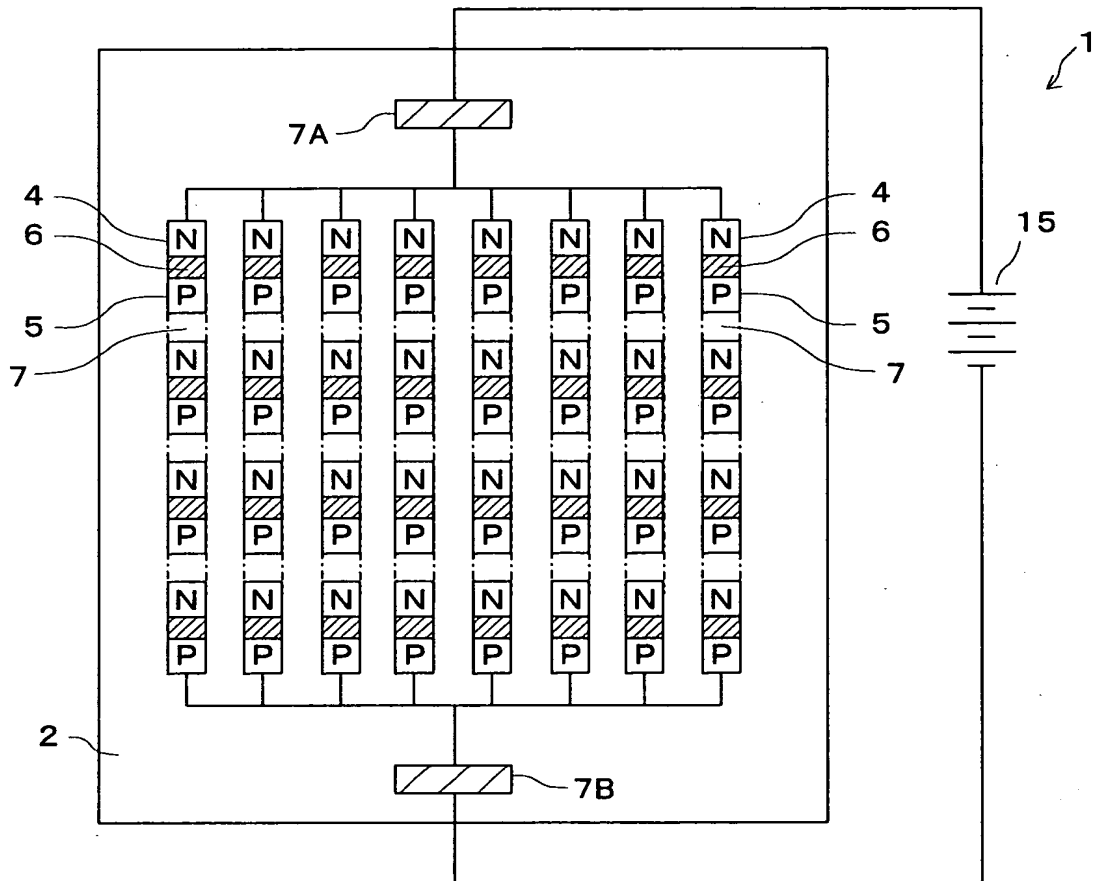


FIG.4

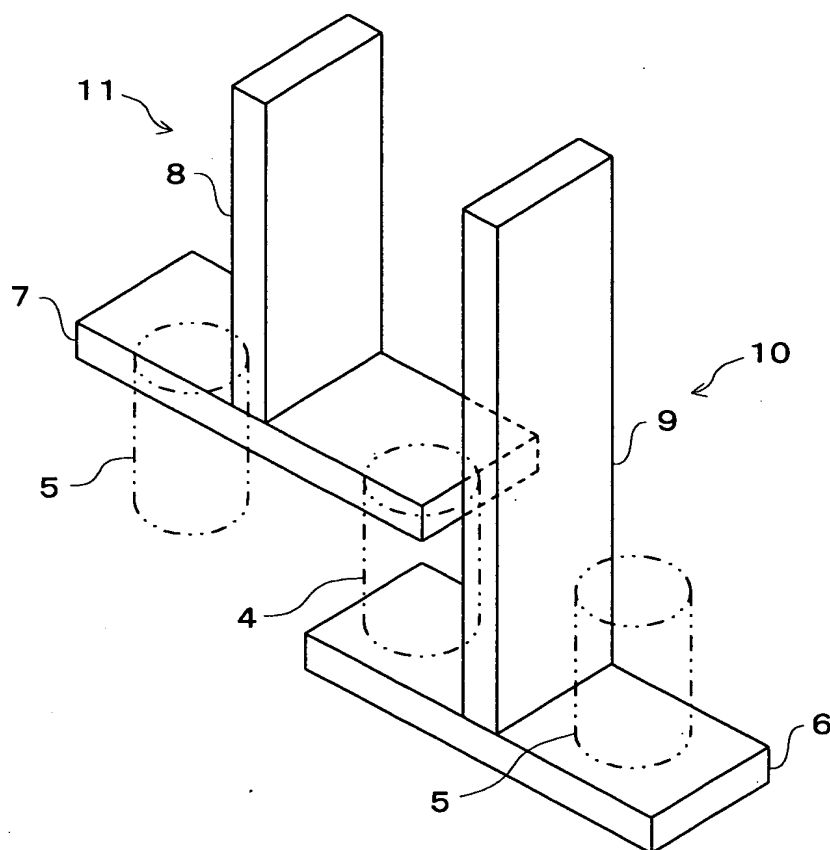


FIG.5

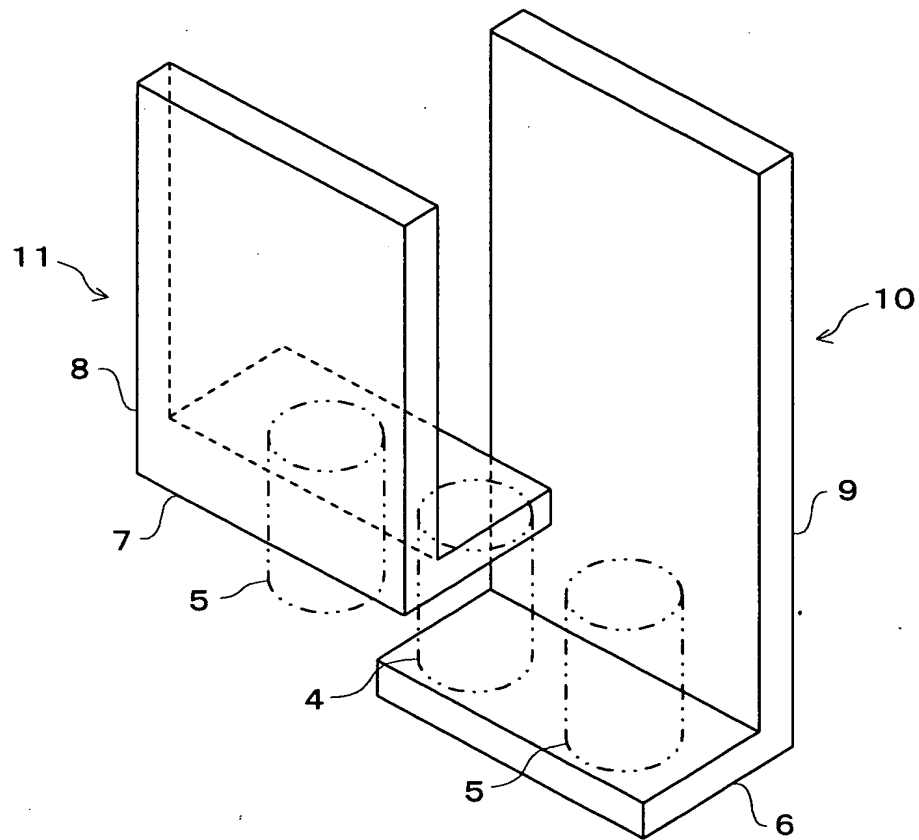
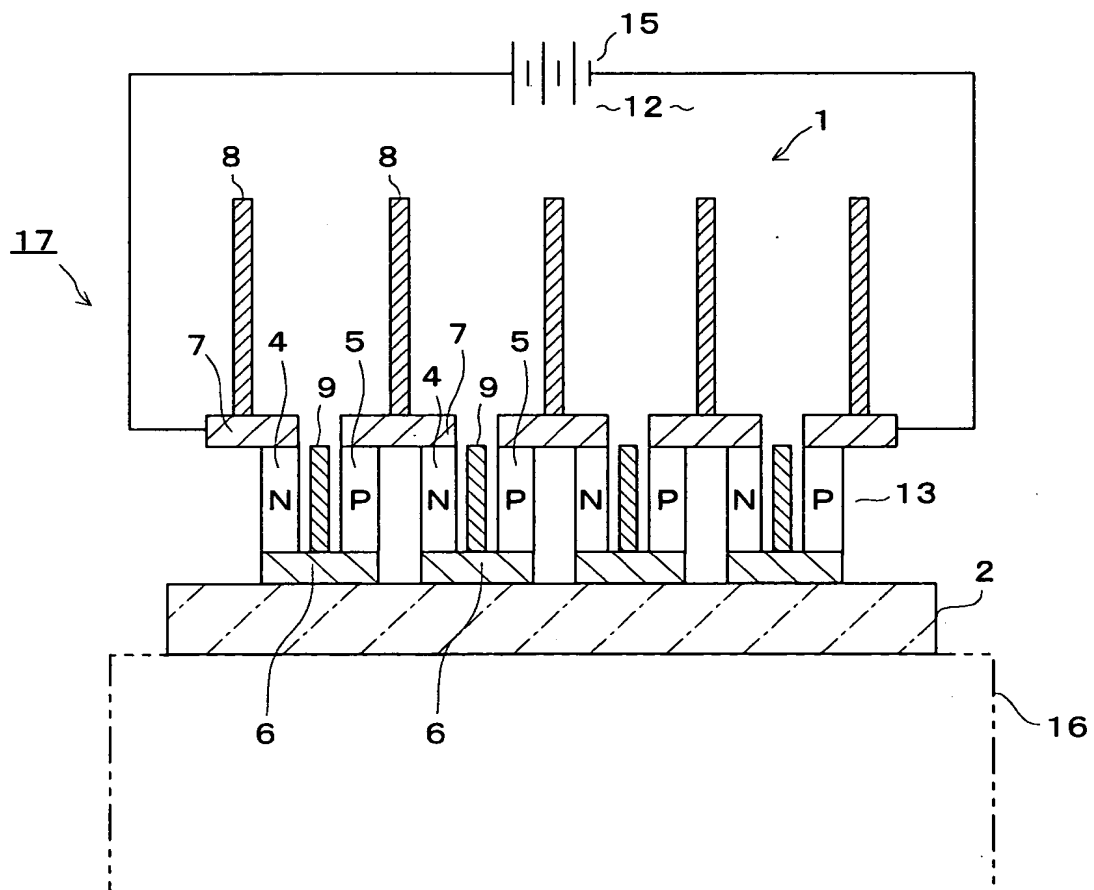


FIG. 6



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FIG. 7

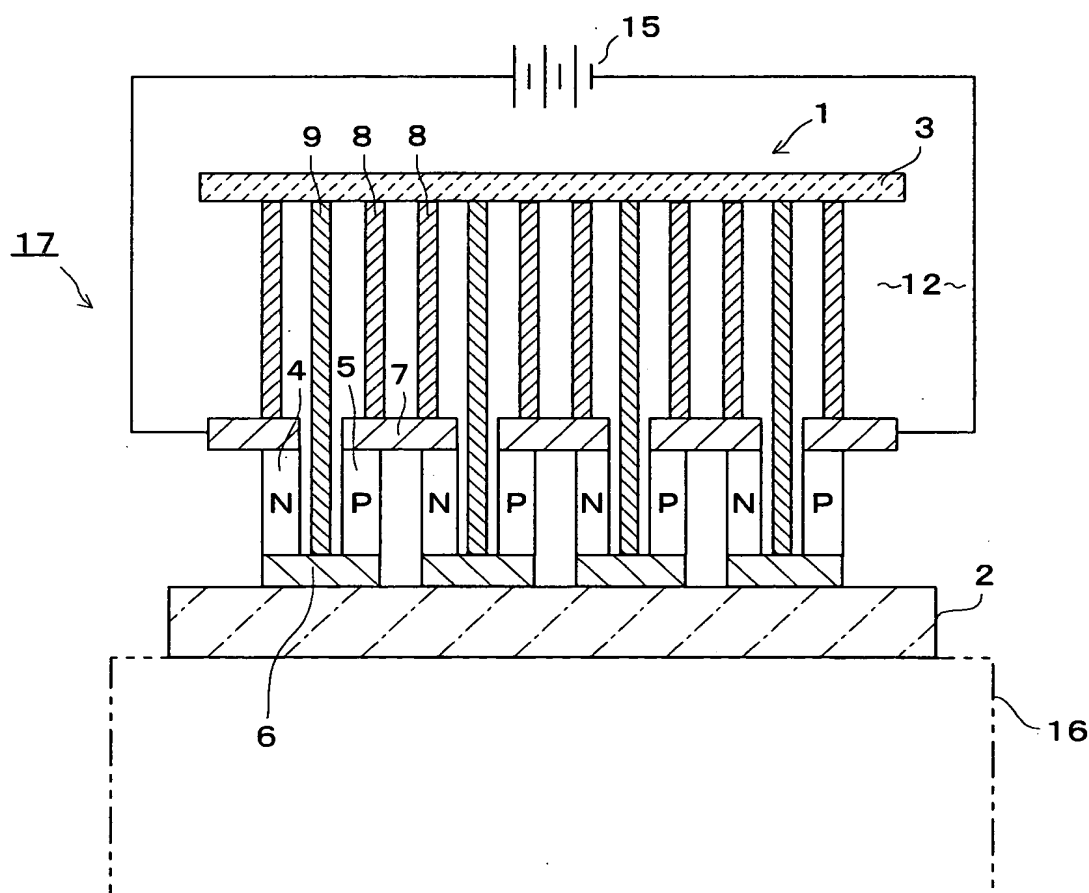


FIG.8

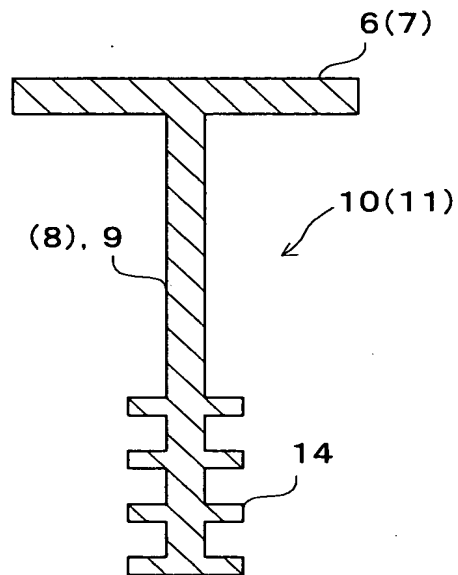




FIG.9

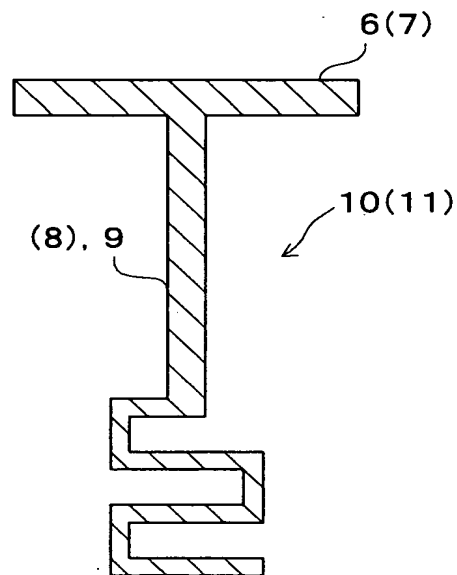


FIG.10

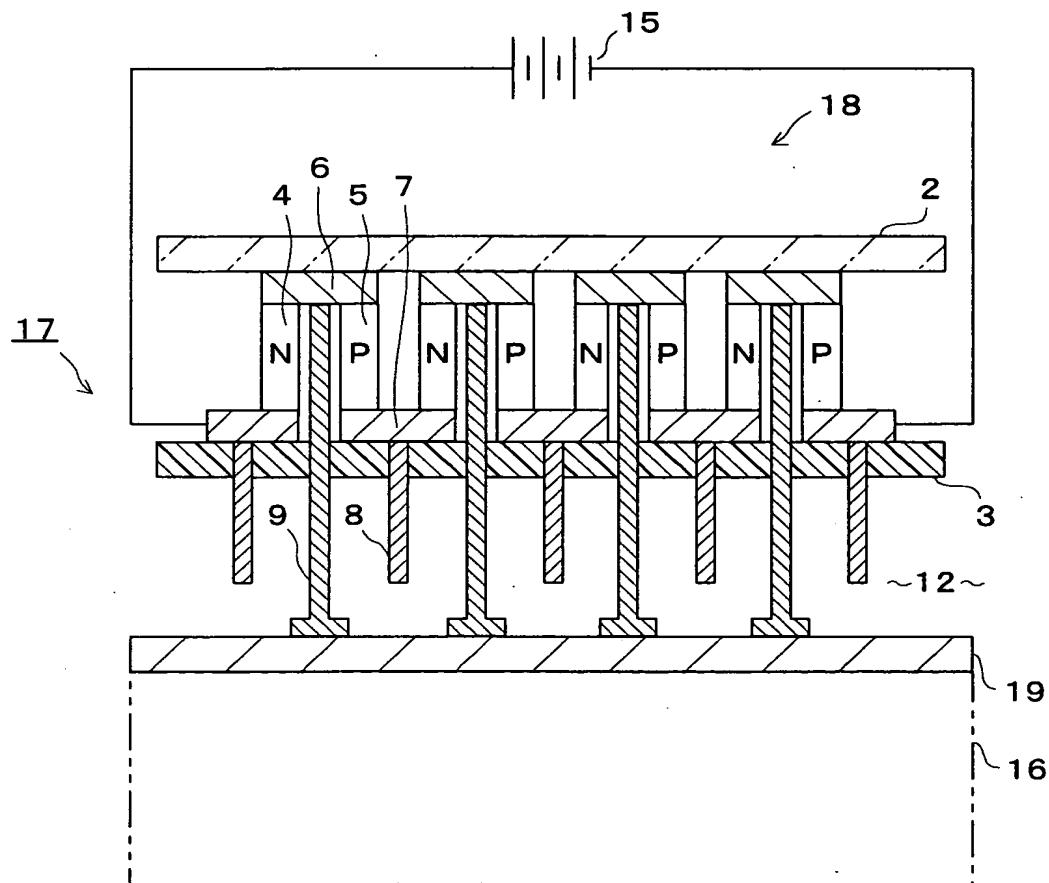


FIG. 11

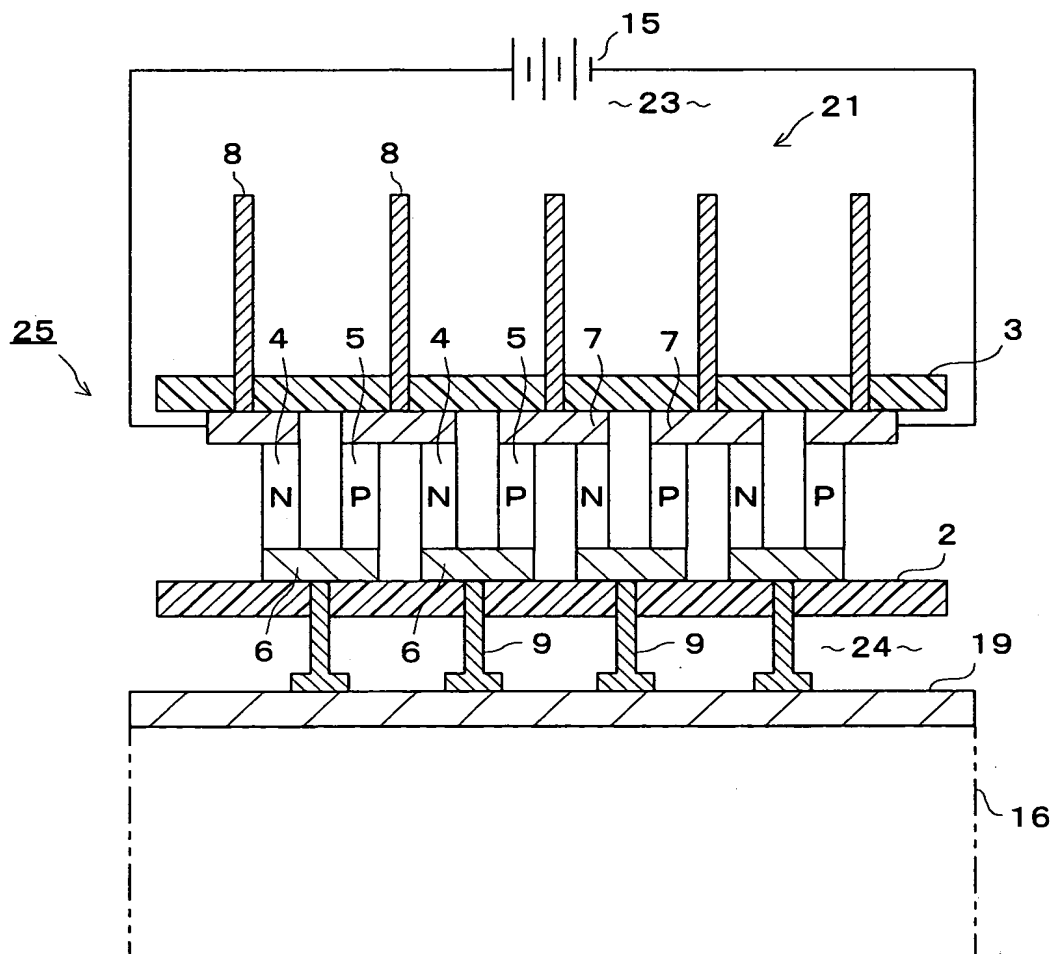
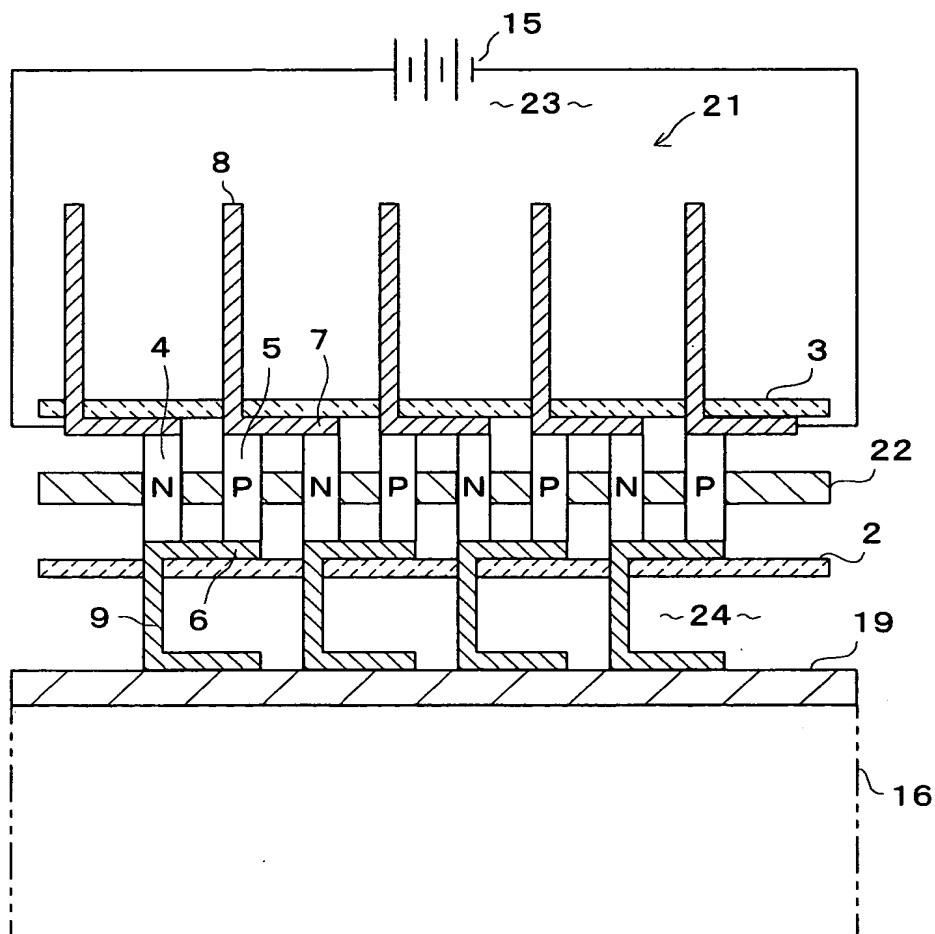


FIG.12



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FIG.13

